Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	612	(photosensitive or lithographical$3) and (optical adj coupler)	US-PGPUB; USPAT	OR	ON	2005/07/19 14:03
L2	114	1 and (three adj dimensional)	US-PGPUB; USPAT	OR	ON	2005/07/19 14:03
L3	52	2 and @ad<"20010919"	US-PGPUB; USPAT	OR	ON	2005/07/19 14:07
L4	16	3 and barrier	US-PGPUB; USPAT	OR	ON	2005/07/19 13:35
L7	0	4 and (conducting adj polymer)	US-PGPUB; USPAT	OR	ON	2005/07/19 13:35
L8	10	4 and (polymer)	US-PGPUB; USPAT	OR	ON	2005/07/19 13:35
L9	470	(photosensitive or lithographical$3) and (optical adj coupler)	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/19 14:03
L10	0	9 and (three adj dimensional)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/19 14:04
L11	0	9 and barrier	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/19 14:04
L12	62	(multi adj (level or layer)) same (optical adj coupler)	US-PGPUB; USPAT	OR	ON	2005/07/19 14:07
L13	49	12 and @ad<"20010919"	US-PGPUB; USPAT	OR	ON	2005/07/19 14:07
L14	35	13 not 3	US-PGPUB; USPAT	OR	ON	2005/07/19 14:08

DOCUMENT-IDENTIFIER: US 20020097962 A1

TITLE: Single and multilayer waveguides and fabrication process

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Cross Reference to Related Applications Paragraph
- CRTX (1):
[0001] This application is a continuation-in-part application of copending application having Ser. No. 09/574,422, filed May 19, 2000, and entitled "**Three-Dimensional**-Opto-Electronic Modules with Electrical and Optical Interconnections and Methods for Making."

Summary of Invention Paragraph - BSTX (4):
[0007] With the increase in clock rates and I/O counts of processing systems implemented on interconnection substrates, the problems of interconnection bottlenecks, noise, signal attenuation, heat generation, and maintaining synchronizable connection lengths in the electrical connections of such systems are appearing. An optical interconnect has the advantage of low RC delay, low signal attenuation, predictable delay, low power, low noise and high tolerance to opens and shorts. However, there is a large **barrier** which prevent optical interconnections from being used in high-speed digital/analog systems. Thus far, bulky driver chips and amplifier chips have been required to provide the conversions between the optical signals in the optical interconnects and the electrical signals which are generated and used by the electronic chips. Each electrical signal that is to be convey optically over a long distance requires a light emitting device, a driver chip to generate the electrical power for switching the light-emitting device at one end of the optical connection. At the receiving end of the optical connection, a photo-detector device and an amplifier is required to convert the optical signal to electrical form. The amplifier is needed because the light power becomes small at the photo-detector device due to considerable loss in conventional optical paths. The driver and amplifier components require space on the circuit substrate, and therefore represent **barriers** to using large numbers of optical connections in a substrate, like a multichip module. In fact, the area needs of these components, as well as the area needs for the emitter devices and photo-detector devices, would increase the size of the module substrates to be larger than module substrates with pure electrical connections. These excess components and their assembling increase manufacturing costs. Furthermore, the

conventional optical connections have longer delay due to EO and OE conversions, which would not provide significant speed benefits over pure electrical modules.

Summary of Invention Paragraph - BSTX (8):
[0010] Another aspect of the present application realizes device and/or material integration into an "opto-electronic (OE) layer", which increases room for chip-mounting, and reduces the total system cost by eliminating the difficulty of optical alignment between OE devices and optical waveguides. OE devices can be embedded into waveguide layers by using wafer processing techniques according to the present invention. Methods according to the present invention enable opto-electronic devices (e.g., modulators, VCSELs, photo-detectors, optical switches, laser-diode (LD), driver chips, amplifier chips, etc.) to be integrated with optical waveguides in ultra thin **polymer** layers on the order of 1 .mu.m to 250 .mu.m.

Summary of Invention Paragraph - BSTX (14):
[0016] Another aspect of the present application is to provide **three-dimensional** opto-electrical modules, and methods for making, which provide for Z-direction waveguides formed perpendicular to the plane of a stack of OE, waveguide, and chip layers, and which interconnections between the Z-direction waveguides and waveguides in the stack of layers.

Brief Description of Drawings Paragraph - DRTX (17):
[0034] FIGS. 71-73 illustrate **three-dimensional** MCM systems according to the present invention.

Brief Description of Drawings Paragraph - DRTX (20):
[0037] FIGS. 90-104 show perspective views of an exemplary waveguide layer being processed according to exemplary methods for forming vertical and horizontal **optical couplers** according to the present invention.

Brief Description of Drawings Paragraph - DRTX (23):
[0040] FIGS. 109-111 show schematic side views of additional **three-dimensional** OE stack configurations according to the present inventions.

Brief Description of Drawings Paragraph - DRTX (34):
[0051] FIG. 129 shows a top plan view of the **polymer** layer in the embodiment

of FIG. 128 which has an opto-electronic device embedded therein according to the present invention.

Brief Description of Drawings Paragraph - DRTX
(47):
[0064] FIGS. 154-158 illustrate an additional embodiment of the **three-dimensional** electro-optical systems according to the present invention.

Brief Description of Drawings Paragraph - DRTX
(48):
[0065] FIGS. 159 and 160 illustrate two methods for constructing holding blocks of the **three-dimensional** electro-optical systems according to the present invention.

Brief Description of Drawings Paragraph - DRTX
(49):
[0066] FIGS. 161-169 illustrate additional, but related, embodiments of the **three-dimensional** electro-optical systems according to the present invention.

Brief Description of Drawings Paragraph - DRTX
(50):
[0067] FIGS. 170-176 illustrate an additional method of constructing opto-electronic/chip layers and opto-electronic waveguide layers for **three-dimensional** modules according to the present invention;

Brief Description of Drawings Paragraph - DRTX
(51):
[0068] FIGS. 177-181 illustrate yet an additional method of constructing opto-electronic/chip layers and opto-electronic waveguide layers for **three-dimensional** modules according to the present invention;

Brief Description of Drawings Paragraph - DRTX
(122):
[0139] FIG. 333 is a perspective view of the improved **optical coupler**;

Brief Description of Drawings Paragraph - DRTX
(124):
[0141] FIG. 335 is a perspective view of another embodiment of an **optical coupler**;

Brief Description of Drawings Paragraph - DRTX
(131):

[0148] FIG. 342 is a top plane view of a conventional **optical coupler**;

Brief Description of Drawings Paragraph - DRTX (132):
[0149] FIG. 343 is a vertical sectional view through the conventional **optical coupler** of FIG. 342;

Brief Description of Drawings Paragraph - DRTX (133):
[0150] FIG. 344 is a top plane view of one embodiment of the improved **optical coupler** of the present invention;

Brief Description of Drawings Paragraph - DRTX (134):
[0151] FIG. 345 is a vertical sectional view through the improved **optical coupler** of FIG. 344;

Brief Description of Drawings Paragraph - DRTX (135):
[0152] FIG. 346 is a top plane view of another embodiment of the improved **optical coupler** of the present invention;

Brief Description of Drawings Paragraph - DRTX (136):
[0153] FIG. 347 is a vertical sectional view through the improved **optical coupler** of FIG. 346;

Brief Description of Drawings Paragraph - DRTX (139):
[0156] FIGS. 350-373 are schematic diagrams representing various process steps for producing the improved optical corner turners and the improved **optical couplers**;

Detail Description Paragraph - DETX (10):
[0171] Switch 26c is embedded in active layer 20, with its bottom surface against the top surface of base substrate 12. There are a number of different types of opto-electronic switch devices that can be used. Such examples are an internal total-reflection switch, a Mach-Zehnder modular, a digital switch, grating-type switch, electro-absorption (EA) light modulator, semiconductor optical gate switch, etc. The exemplary switch device shown in FIG. 2 is an internal total-reflection switch, and it comprises a body of electro-optical (EO) material 626 which changes its refractive index when an electric field is

applied across it. Referring to FIG. 3, the body of EO material 626 is formed in a Y-shaped body having a through section between waveguide 24c and a second output waveguide 24i, and a branch section from this through section to output waveguide 24h. Material 626 is placed in the path between input waveguide 24c and output waveguides 24h and 24i, and is positioned between cladding layers 21 and 23. The field is applied by two opposing electrodes 27, which also serve as the electrical terminals of the device. Short electrical traces, which are not present in the cross-sectional plane of FIG. 2, connect electrodes 27 to respective connection pads 32, which are not present in the cross-sectional plane of FIG. 2 but whose locations in back of the plane are shown by dashed lines. When no potential is applied across electrodes 27, light travels along the through section from waveguide 24c to waveguide 24i. When an electrical potential difference is applied between electrodes 27, a portion of the EO material 626 undergoes a change in its index of refraction, which in turn changes the propagation direction of the light so a major portion of the light goes into the output waveguide 24h. More specifically, the light encounters a lower index of refraction at the section of EO material 626 located between electrodes 27, and is reflected to the branch section. EO material 626 may comprise organic materials, including electro-optic **polymers,** such as those disclosed in U.S. Pat. No. 5,444,811, assigned to the assignee of the present application and incorporated herein by reference. EO material 626 may also comprise multiple quantum well devices and quantum dots made from exemplary III-V compounds, such as Al.sub.xGa.sub.1-xAs/Al.sub.yGa.sub.1-yAs. When applying a reverse voltage bias, these devices are able to change their indices of refraction as a function of the applied bias.

Detail Description Paragraph - DETX (21):

[0182] FIG. 9 shows a partial cross-sectional view of a second exemplary light-emitter device 36b', and FIG. 10 shows a top plan view of device 36b' in relation to waveguide 24h. Device 36b' comprises a vertical cavity surface emitting laser (VCSEL) 638 formed on a semiconductor mini-chip (or die) 636. The VCSEL element 638 generates light which is directed perpendicular to the top surface of mini-chip 636, which is different from the previous example where the light was generated at a side of the mini-chip. Substrate 636 lies below core layer 24, and a mirror 639 is positioned in front of VCSEL element 638 to reflect the vertical light beam of element 638 into waveguide 24h, and thereby along a horizontal direction. The surface of mirror 639 is preferably at a 45.degree. angle to the element's light beam. One end of optical waveguide 24h is located over VCSEL element 638 and is beveled at an angle (preferably at a 45.degree. angle) with respect to the normal vector of the substrate surface. (The normal vector is the vector which is perpendicular to the top surface of base substrate 12). The beveling may be accomplished by

laser abrasion using a laser that is tilted at a 45.degree. angle with respect to the normal vector of the substrate surface. Reactive ion etching (RIE) methods may also be used. If **photosensitive** materials are used, tilted lithographic exposures may be used. Mirror 639 is built upon the beveled surface, such as by depositing a reflective metal or reflective material over this area. Exemplary reflective metals include silver (Ag), aluminum (Al), gold (Au), copper (Cu), chromium (Cr), tungsten (W), titanium (Ti), etc., and exemplary reflective materials include multilayer dielectric coatings comprising such materials as titanium dioxide (TiO.sub.2), silicon dioxide (SiO.sub.2), alumina (aluminum oxide Al.sub.2O.sub.3), zinc oxide (ZnO), chromium oxide (Cr.sub.2O.sub.3). The angle of mirror 639 may vary from a value of 45.degree. by small amounts, depending upon the difference in the index of refraction of the core and cladding layers. If the difference in the indices of refraction is .DELTA.n=0.02, then a maximum angle deviation of .+-.3.degree. can be tolerated. Given the value of .DELTA.n, it is well within the skill of the art to compute the maximum angle deviation. As used herein, a 45.degree. angle or an angle of approximately 45.degree. compasses all angles within the angle tolerance for the corresponding value of .DELTA.n; thus angles from 42.degree. to 48.degree. are encompassed for a .DELTA.n of 0.02, which has the above angle tolerance of .+-.3.degree.. Instead of mirror 639, an optical grating may be used. An optical grating may comprise a sequence of material layers having alternating indices of refraction n.sub.1 and n.sub.2 and being formed at a 45.degree. angle to the substrate normal vector. Such an optical grating may be constructed by forming a set of spaced cuts in the end of waveguide 24h, and then filling the cuts with an optical material having a different index of refraction.. The set of 45.degree. angle cuts is most readily obtained by using a **photosensitive** optical material and passing the exposure radiation through a optical device which generates an interference pattern which has closely spaced, alternating regions of high and low intensity light. The interference pattern is tilted at an approximate 45.degree. angle to the normal vector of the substrate and focused on the region where the grating is to be formed. As in the mirror case, small angle deviations can be tolerated, and the tolerance can be computed from the indices of refraction by those of ordinary skill in the optics art. The gratings may also be formed by anisotropic etching methods which are described in greater detail below with reference to the devices illustrated in FIGS. 22-25.

Detail Description Paragraph - DETX (24):
[0185] Referring to FIG. 11, a bottom electrode 27 of switch device 26 is formed on the top surface of base substrate 12 by conventional deposition and photo-lithographic steps that are well known to the art. In addition to forming electrode 27, alignment marks for further processing steps may be

formed, or these alignment marks may be etched in the surface of base substrate 12 prior to forming electrode 27. As the next step, cladding layer 21 is formed, such as by spin-coating a fluidized **polymer** over base substrate 12. In order to attach components 28, a material for layer 21 is selected which has adhesive capabilities, such as Hitachi's fluorinated polyimide OPI-N1005 or a solvent-free (non-gaseous) epoxy materials. The thickness of layer 21 may range between 1 .mu.m and 20 .mu.m, after any shrinkage from a subsequent curing step.

Detail Description Paragraph - DETX (27):
[0188] As indicated above, the thickness of the individual components (e.g., 28) is preferably relatively thin, such as on the order of 1 .mu.m to 20 .mu.m. Such thin O/E components can be manufactured using the vapor phase epitaxial liftoff process described by Yablonovitch, "Vapor Phase Epitaxial Liftoff Process of GaAs", the Fall 1997 Materials Research Symposium. Other processes, such as liquid phase epitiaxial liftoff or polishing may also be used as well. The epitaxial lift-off (ELO) process takes advantage of the very large difference in etch rate between GaAs (Gallium Arsenide) and AlAs (Aluminum Arsenide), or between GaAs and Al.sub.xGa.sub.1-xAs (Aluminum Gallium Arsenide) with large x, in hydrofluoric acid. Starting with a GaAs substrate, a layer of AlAs is formed over the top surface by epitaxial growth (e.g., MBE, OMVPE, etc.). Layers of GaAs and Al.sub.xGa.sub.1-xAs are then formed over the AlAs layer, also by epitaxial growth. Opto-electronic devices are then formed in the top GaAs layer, including electrodes and a top passivation layer. (For the present invention, a polish-stop layer is formed on top of the passivation layer and electrodes, as described below). Deep trenches are then formed in the top GaAs layer to separate the devices into individual components or individual array chips (which are chips containing multiple devices). (Such array chips are usefully in implementing optical buses where multiple signals are grouped together and routed from a bank of optical switch devices (or emitters) to a bank of photo-detectors.) As a supporting substrate, a **polymer** film, such as Mylar, or glass, quartz, is then laminated to the top surface of the GaAs components, including the array chips. The entire substrate is the exposed to a hydrofluoric acid etch, which etches the AlAs layer laterally and results in the release of the GaAs and Al.sub.xGa.sub.1-xAs components (e.g., mini-chips) from the GaAs substrate while still being attached to the **polymer** film (when a **polymer** is used for the supporting substrate). The components may then be cut from the **polymer** film, or they may be held by the film until used. In the latter case, layer 21 is soft-baked to a point where it has more tacky adhesion force than the laminated **polymer** film; when the component is pressed in the tacky layer 21, it is retained on layer 21 when the laminated **polymer** film is pulled away, and it separates from the **polymer** film. As another